Design and Implementation of 32 Bit ALU Using Look Ahead Clock Gating Logic

D.Nirosha
PG Scholar,ME VLSI Design, PSNACET, India.

T.Thangam
Associate Professor ECE, PSNACET, India.

Abstract – Any type of digital architecture is modified by using the VLSI technology. In digital systems, clock gating is the best method to reduce consumption of power. As power consumption plays an important role in any integrated circuit. This methodology is mainly used in all type of real world applications and this technology is to enhance the internal architecture level. There are 3 gating methods. The most popularly known gating method is synthesis based. Unfortunately, the Synthetic based gating method leaves the majority of the clock pulses driving the flip flops are terminated. A data driven method halts most of the clock pulses and produces higher power savings, but its application is complex and dependent. The Auto-Gated Flip Flops (AGFF) is the third method which yields moderately lower power saving. This paper introduces a novel Look-Ahead Clock Gating (LACG) method which is the combination of all the three gating methods. It calculates the clock enabling signals of every flip flops one cycle from this time, which it depends on the FFs cycle data at present. In a CPU, the most commonly edited modules are the ALU. During most instruction executions, it is employed. Therefore, a major concern in the ALU is the consumption of power. This paper motivates to reduce the ALU architecture for many digital applications and to improve the internal process in ALU architecture with look ahead clock gating approach. Reduction of delay and power for the data path PE unit in 32 bit ALU architecture.

Index Terms – ALU, LACG, Clock gating, dynamic power.

1. INTRODUCTION

In the earlier days, the designers of VLSI were more interested on the area of the circuits, performance, reliability and cost was also the main consideration and power consumption was their minor consideration. Now-a-days, the power is also being given equal importance in comparison to area and speed. The dynamic power dissipation is being comparable with both short circuit and leakage power as technology scale down. To identify and modify the various leakages and switching of components is very essential to estimate and also the reduction of power consumption in high speed and low power applications. Clock gating is the best method to reduce the power consumption. It is involved in all levels of system architecture, logic design, block design and gates. The predefined enabling signals and gating signal are ANDed. There are three gating methods, first one is the synthesis based, which enables clock signals based on the logic of the fundamental system. Unfortunately, it leaves the majority of the clock pulses driving the flip flops are terminated. Second is the data driven method which stops most of those clock pulses and gains higher power savings, but it is application dependent and the implementation is highly complex. And the third method is auto gated flip flop. It is simple but gains relatively small power savings. In synthesis based clock gating, functional blocks and modules are not needed to be clocked as the clock enabling signals are well understood the system level. It can be defined effectively and capture the period. To address the redundancy from the synthesis based, a data driven clock gating is proposed for flip flops. If the flip flops state is not changed to the next clock cycle then the flip flops driven by the clock signals are disabled. It suffers from a very short time window where the gating circuitry works correctly. The delay of the XOR, OR, AND gate and latch need not beyond the setup time of the flip flop. Another difficulty of data driven clock gating is its design methodology. The low power look ahead clock gating method combines all the three gating methods. The system clock signals is one of the main dynamic power consumers in computing and electronic products, which is normally responsible for 30-70 % of the total dynamic switching power consumption. Several techniques are introduced to reduce the dynamic power of which clock gating is primary. This look ahead clock gating calculates the clock enabling signals of every flip flops one cycle from this time, which it depends on the FFs cycle data at present. For computing the enable signals and the propagation, a full clock cycle is allotted for both auto gated and data driven in order to avoid its tight timing constraints. This look ahead clock gating method is introduced, based on the auto gated flip flop. The Comparison of the look ahead, power gating and data driven clock gating are done in this paper. It shows, when compared to the data driven, the look ahead consumes less power and to reduce the power.

2. ARCHITECTURE

The ALU architecture mainly used to perform the arithmetic and logical process and the arithmetic process consists the adder and subtractor and multiplier architecture. The mux input

section to change the output based on selection process. The selection process used to modify the output unit architecture. The ALU block is used to optimize the internal architecture. The internal architecture to consume the three arithmetic operations and five logical operations. The buffer architecture used to store the output with delay time for the ALU operation and to check the required selection signal .The mux operation used to find the output and to store the mux input. And to select the input selection signal and to display the output result.

3. MODULES

3.1. Selection Mux Architecture

The input bits are to be applying the ALU circuit. The 8:1 mux is used to select the operation output data bits based on arithmetic and logical operation. The mux architecture consists of overall internal ALU architecture output data bits and the look ahead clock gating technique is used to optimize the selection process time. The mux input section is to change the output based on selection process. The selection process is used to modify the output unit architecture.

3.2. Alu Architecture

The ALU architecture mainly used to perform the arithmetic and logical process and the arithmetic process consists the adder and subtractor and multiplier architecture. The logical process consists the AND gate and OR gate and XOR gate and inverter gate architecture. This architecture is to design the structure methodology. The ALU architecture used to all type of core process and to optimize the internal architecture.

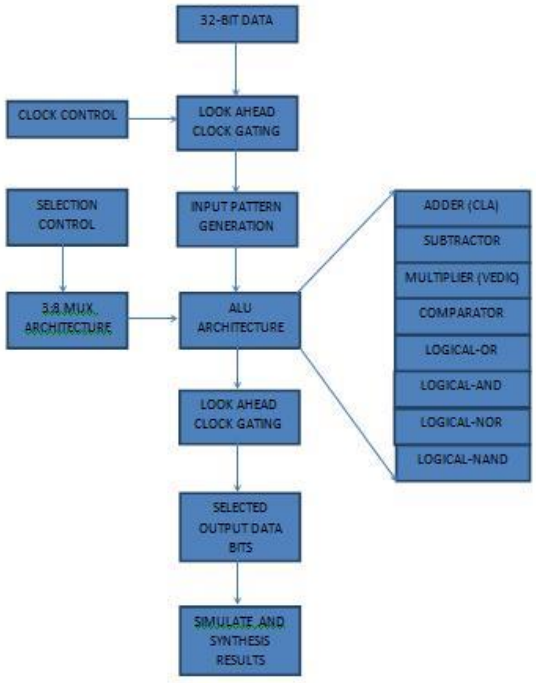

Figure 1 Flow Diagram of ALU Architecture

3.3. Alu Internal Block

The ALU block to optimize the internal architecture. The internal architecture is to consume the three arithmetic operation and five logical operations. The arithmetic operation requires more time and high path delay and reduce the speed. So the modification process mainly focused by the carry propagation process. So we use the carry selection adder architecture function in addition operation and the multiplier operation.

3.4. Look Ahead Clock Gating

The look ahead clock gating circuit takes an input clock signal and generates a gated clock based on a control signal. The look ahead clock gated clock signal is used to activate the arithmetic or logic or shift unit. It prevents unnecessary charging and discharging of the clock signal in inactive modules which leads to lower dynamic power dissipation. Look ahead clock gating technique is a power down methodology, which involves selectively clocking modules as and when required while keeping other inactive modules in sleep mode.

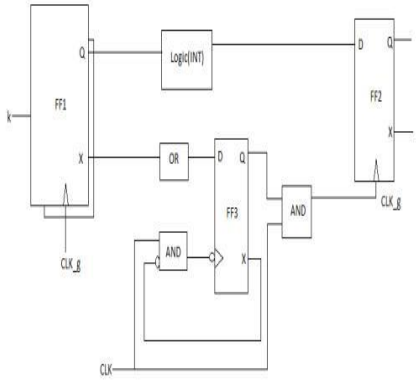

Figure 2 Block Diagram of Look Ahead Clock Gating

4. EXPERIMENTAL RESULTS

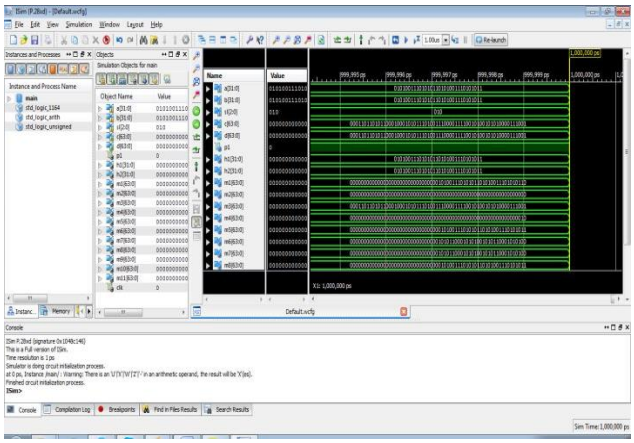

Figure 3 Simulation Results

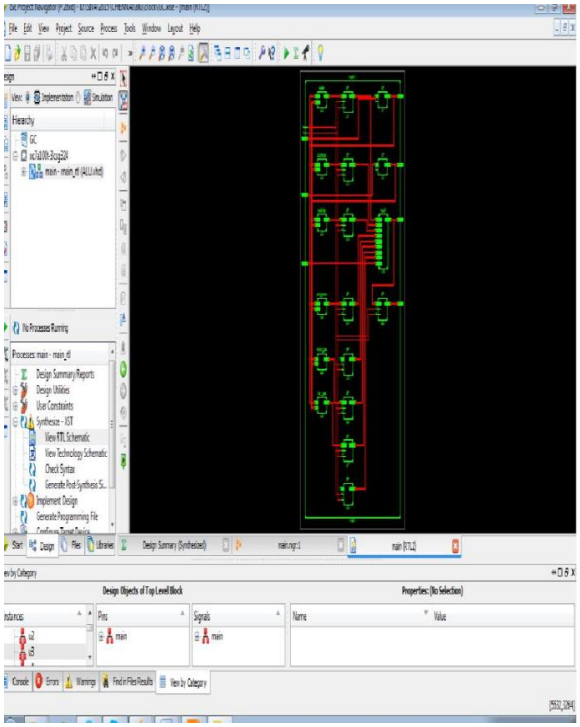

Figure 4. RTL Diagram of 32 Bit ALU

5. POWER ANALYSIS

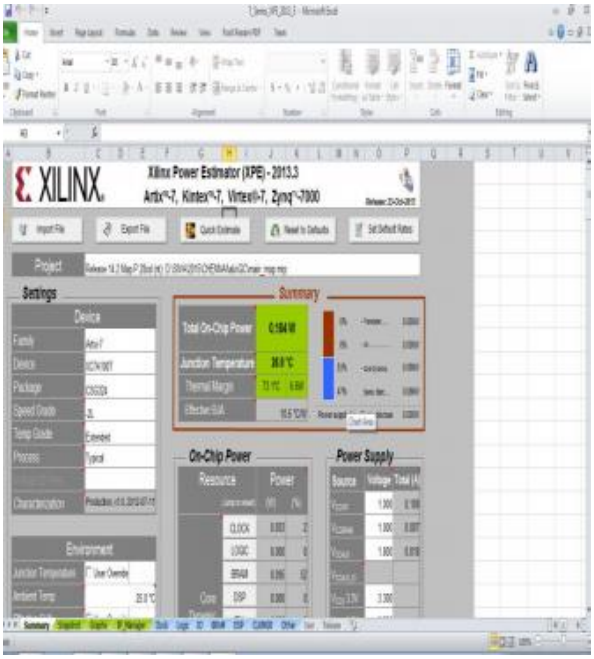

Figure 5. Power Analysis of 32 Bit ALU Using Clock

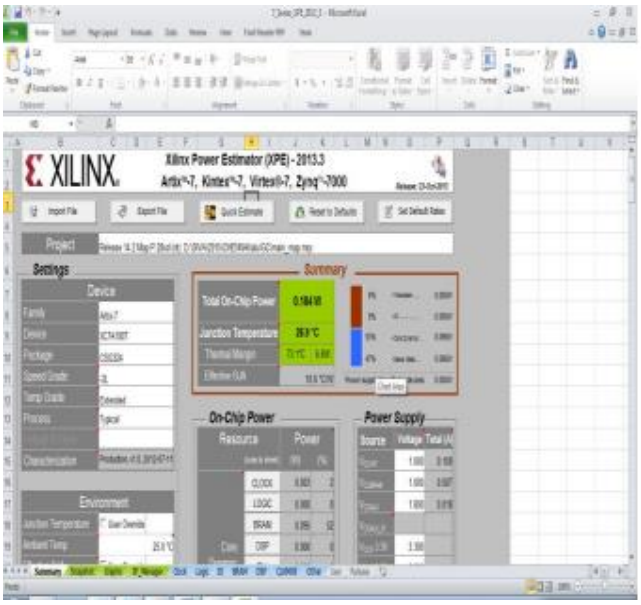

Figure 6. Power Analysis of 32 Bit ALU Using Look Ahead Clock Gating Technique

	32-BIT ALU WITH CLOCK	32-BIT ALU WITH LOOK AHEAD CLOCK GATING
BIO COUNT	197	131
DELAY TIME (ns)	1.050	1.005
LATENCY TIME (ns)	0.672-1.149	0.619-1.253
TOTAL POWER (mW)	233	184
DYNAMIC POWER (mW)	147	98

Table.1 Comparison between Clock and Look Ahead Clock Gating

6. CONCLUSION

In this paper, a low power look ahead clock gating is presented and compared it with the previously clock gating technique i.e. the data driven clock gating and with clock. It is also very useful in reducing the dynamic power. One of the major sources responsible for power consumption in digital circuits is the systems clock signal. It contributes towards a large amount of power consumption. This look ahead clock gating technique is very much useful for reduction of the power consumption in

digital systems. As it computes each flip flop clock enabling signals per cycle ahead of time. It is based on the flip flop present cycle data and the drawbacks of the three gating methods have been overcome. The result shows minimum power consumption than that of data driven clock gating. In this paper, a 32 bit ALU is designed and implemented on Xilinx FPGA using VHDL. ALU is the part of a computer that performs all arithmetic operations, such as addition and subtraction, decrement, increment, shifting and all kinds of basic logical operations.

REFERENCES

[1] S. Wimer, "On optimal flip-flop grouping for VLSI power minimization," Oper. Res. vol.4, no . 5,pp. 486-489, sep. 2013
[2] J. A. Kathuria, M. Ayoub, M.Khan, and A.Noor, " A review of clock gating Technique," MIT Int. J. Electron. And Commun. Engin., vol.1, no.2,pp.106-114, Aug. 2011
[3] A.G.M. Strollo and D. De Caro," Low power flip flop with clock gating on master nad slave latches," Electro. Lett., vol. 36, no.4, pp.294-295, Feb.2000.
[4] S.Wimer and I.Koren, "The optimal fan-out of clock network for power minimization by adaptive gating," IEEE Trans. VLSI Syst., vol. 20, no. 10, pp.1772-1780, Oct.2012.
[5] K. Madhanmohan, R.Murugasami," Dual Optimized System for Flip-Flop Grouping Data Driven Clock Gating Approach," International Journal of Advanced Reasearch in computer science and software engineering, vol. 4, issue 4, april 2014
[6] V. G. Oklobdzija, Digital System Clocking- Highperformance and Low-power Aspects, New York, NY, USA: Wiley, 2003.
[7] L. Benani, A. Bogliolo, and G. De. Micheli, " A survey on design techniques for system-level dynamic power management". IEEE Trans. VLSI Syst., vol. 8, no. 3, pp. 299- 316, jun. 2000.